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CLAIMS

1. A method of controlling the bias voltage of an avalanche photodiode in an optical communications system including forward error correction, the method comprising measuring the error rate in an electrical signal converted from an optical signal by the avalanche photodiode, and adjusting the bias voltage applied to the avalanche photodiode to minimise the error rate in the electrical signal, wherein the error rate is measured over a plurality of sample periods and a determination is made of whether or not the error rate is increasing or decreasing with time.

2. A method according to claim 1, wherein the bias voltage is determined by the value of a counter which is incremented or decremented every sample period, comprising changing the count direction of the counter if the error rate is increasing with time.

3. A method according to claim 2, comprising inhibiting movement of the clock if the error rate is zero.

4. A method according to claim 2 or claim 3, wherein the sample period is determined by a clock tick.

5. A method according to claim 4, wherein the interval between clock ticks is variable.

6. A method according to claim 5, wherein the interval between clock ticks varies in dependence on the measured error rate.

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7. A method according to claim 5 or claim 6, comprising a plurality of possible interval lengths, wherein the interval selected is increased if the error rate is below a first level and decreased if the error rate is above a second level.

8. Apparatus for controlling the bias voltage of an avalanche photodiode (APD) in an optical communications system including forward error correction (FEC), comprising an error rate measurer for measuring the error rate in an electrical signal converted from an optical signal by the APD, and an adjustment circuit for adjusting the bias voltage applied to the APD to minimise the measured error rate, wherein the adjustment circuit comprises decision logic for determining whether the error rate is increasing or decreasing with time.

9. Apparatus according to claim 8, wherein the adjustment circuit comprises a counter, the value of which determines the level of the bias voltage, and means for changing the count direction if the decision logic determines that the error rate is increasing.

10. Apparatus according to claim 9, wherein the means for changing the count direction is a toggle.

11. Apparatus according to claim 10, comprising a digital to analog converter for converting the counter value to an analog APD bias voltage.

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12. Apparatus according to any of claims 8 to 11, wherein the adjustment circuit comprises an error pulse counter for counting error pulses over a predetermined interval, and a store for holding error counts for a plurality of earlier intervals.

13. Apparatus according to claim 12, wherein the decision logic operates on the error counts held in the store.

14. Apparatus according to claim 12 or 13, comprising means for varying the interval over which error pulses are measured.

15. Apparatus according to claim 14, wherein the interval changing means varies the interval in dependence on the error rate.

16. Apparatus according to claim 14 or 15, wherein the interval varying means varies the interval between one of a plurality of different interval lengths.

17. Apparatus according to any of claims 9 to 11, comprising an inhibitor for inhibiting movement of the counter if the measured error rate is zero.